WHAT IS CLAIMED IS

1. A system for transmitting data, the system comprising:

(a) at least one bus data line; and

(b) at least one transmitter, each said transmitter including:

(i) for each said at least one bus data line, a respective open-driver bus data line driver, each said open-driver bus data line driver drivingly connected to a corresponding said bus data line.

2. The system of claim 1, wherein said transmitter further includes:

(ii) at least one transmit data line for driving a respective said open-driver bus data line driver.

3. The system of claim 2, wherein said transmitter further includes:

(iii) at least one active-pullup driver drivingly connected to a respective said open-driver bus data line driver.

4. The system of claim 2, wherein each said transmitter further includes:

(iii) a collision-detection mechanism operative to detect a data difference between one of said at least one transmit data line and a corresponding said bus data line, and to set a collision signal upon detecting said data difference.

5. The system of claim 4, wherein said collision signal being set causes said open-driver bus data line driver to drive its respective said bus data line with data selected to cause any said transmitter that is transmitting data to said bus data lines to

detect a collision.

6. The system of claim 4, wherein said collision signal being set causes said open-driver bus data line driver to drive its respective said bus data line to a low logic level.

7. The system of claim 4, further comprising:

(c) a clock signal line,

operative to transmit a clock signal, said clock signal operative to restrict setting of said collision signal only according to data on said transmit data lines and said bus data lines during a predetermined range of times within a period of said clock signal.

8. The system of claim 4, further comprising:

(c) a data-sense signal line operative to conduct a data-sense signal.

9. The system of claim 8, wherein said data-sense signal has a driven state, and wherein each said transmitter further includes:

(iv) an open-driver data-sense signal line driver operative to drive said data-sense signal line to said data-sense signal's driven state when said transmitter is transmitting data.

10. The system of claim 9, wherein said open-driver data-sense signal line drivers of said at least one transmitter are connected in a wired-and configuration.

11. The system of claim 8, further comprising:

(d) a conductor at a high logic level; and

(e) a resistor,

said resistor being connected between said conductor and said data-sense signal line.

12. The system of claim 8, wherein said data-sense signal has a default state, and wherein said transmitter further includes:

(iv) a latch operative, if said collision signal is set, to keep said collision signal set until said data-sense signal is in said default state thereof.

13. The system of claim 4, wherein said transmitter further includes:

(ii) a data-valid signal line,

operative to transmit a data-valid signal, each said open-driver bus data line driver of said transmitter being operative to be in a high-impedance state when said data-valid signal is in an inactive state and said collision signal is cleared.

14. The system of claim 1, further comprising:

(c) a data-sense line operative to conduct a data-sense signal.

15. The system of claim 14, wherein said data-sense signal has a driven state and wherein each said transmitter further includes:

(iv) an open-driver data-sense signal line driver operative to drive said data-sense signal line to said data-sense signal's driven state when said transmitter is transmitting data.

16. The system of claim 15, wherein said open-driver data-sense signal line drivers of said at least one transmitter are connected in a wired-and configuration.

17. The system of claim 14, further comprising:

(d) a conductor at a high logic level; and

(e) a resistor,

said resistor being connected between said conductor and said data-sense signal line.

18. The system of claim 1, further comprising:

(c) a conductor at a high logic level; and

(d) a resistor,

said resistor being connected between said conductor and one said bus data line.

19. The system of claim 1, further comprising:

(c) a clock signal line,

operative to transmit a clock signal to said transmitter.

20. The system of claim 1, further comprising:

(c) a receiver operative to receive data from said bus data lines.

21. The system of claim 20, further comprising:

(d) a clock signal line,

operative to transmit a clock signal to said receiver

22. The system of claim 1, wherein said transmitter further includes:

(ii) a data-valid signal line,

operative to transmit a data-valid signal, each said open-driver bus data line driver of said transmitter being operative to be in a high-impedance state when said data-valid signal is in an inactive state.

23. The system of claim 1, wherein corresponding said open-driver bus data line drivers connected to a corresponding said bus data line are connected in a wired-and configuration.

24. A system to connect a device to a bus, the device having a transmitter and a receiver, the bus having a plurality of bus data lines, the bus being operative to be connected to other transmitters and to other receivers, the system comprising:

(a) for each of the bus data lines, a respective open-driver bus data line driver suitable to be drivingly connected to said each bus data line.

25. The system of claim 24, further comprising:

(b) at least one transmit data line operative to accept data from the transmitter of the device and to drive a respective said open-driver bus data line driver.

26. The system of claim 25, further comprising:

(c) a collision-detection mechanism operative to detect a data difference between one of said at least one transmit data line and the corresponding bus data line, and to set a collision signal upon detecting said data difference.

27. The system of claim 26, wherein said collision signal being set causes at least

one of said plurality of open-driver bus data line drivers to drive its respective bus data line with data selected to cause any transmitter that is transmitting data to the bus data lines to detect a collision.

28. The system of claim 26, wherein said collision signal being set causes at least one of said plurality of open-driver bus data line drivers to drive its respective bus data line to a low logic level.

29. The system of claim 26, further comprising:

(d) a clock signal line,

operative to transmit a clock signal, said clock signal operative to restrict setting of said collision signal only according to data on said transmit data lines and the bus data lines during a predetermined range of times within a period of said clock signal.

30. The system of claim 26, further comprising:

(d) an open-driver data-sense signal line driver operative to drive a data-sense signal line of the bus to a driven state when the transmitter of the device is transmitting data.

31. The system of claim 26, further comprising:

(d) a conductor at a high logic level; and

(e) a resistor,

said resistor being connected between said conductor and said data-sense signal line.

32. The system of claim 26, further comprising:

(d) a latch operative, if said collision signal is set, to keep said collision signal set until said data-sense signal line is in a default state.

33. The system of claim 26, further comprising:

(d) a data-valid signal line,

operative to accept a data-valid signal, each said open-driver bus data line driver of the system being operative to be in a high-impedance state when said data-valid signal is in an inactive state and said collision signal is cleared.

34. The system of claim 24, further comprising:

(b) a conductor at a high logic level; and

(c) a resistor,

said resistor being connected between said conductor and one bus data line, said conductor and said resistor operative to cause said one bus data line to be at a high logic level when all said bus data line drivers connected to said one bus data line are in a high-impedance state.

35. The system of claim 24, further comprising:

(b) a clock signal line,

operative to transmit a clock signal to the transmitter of the device and to the receiver of the device, said clock signal operative to synchronize transmission of data by the transmitter to the bus data lines, and said clock signal operative to synchronize reception of data by the receiver from the bus data lines.

36. The system of claim 24, further comprising:

(b) a gate; and

(c) a data-valid signal line, operative to accept a data-valid signal,

said gate operative to cause one said open-driver bus data line driver of the system to be in a high-impedance state when said data-valid signal is in an inactive state.

37. A method of transmitting data, via at least one bus data line, from a transmitter to a receiver, the transmitter having as many transmit data lines as there are bus data lines, comprising the steps of:

(a) providing an open-driver bus data line driver; and

(b) transmitting data from the transmitter to the receiver via the transmit data line, said open-driver bus data line driver, and the bus data line.

38. The method of claim 37, further comprising the step of:

(c) monitoring the transmit data line and the bus data line for a data difference.

39. The method of claim 38, further comprising the step of:

(d) upon detection of said data difference, retransmitting the data.

40. The method of claim 38, further comprising the step of:

(d) upon detection of said data difference, transmitting data selected to cause any transmitter that is transmitting data to the bus data lines to detect a collision, until no transmitters connected to the bus data line are transmitting data.

41. The method of claim 38, further comprising the step of:

(d) upon detection of said data difference, transmitting a low logic level on the bus data line until no transmitters connected to the bus data line are transmitting data.